

What is claimed is:

1           1.       A semiconductor package comprising:  
2           a semiconductor die having a front side and an opposed backside;  
3           a backside metallization layer formed on the backside of the die;  
4           an integrated heat spreader; and  
5           a thermal interface including a fluxlessly-capable solder portion deposited on a top  
6           surface of the integrated heat spreader and bonded to said metallization layer under load and  
7           heat.

1           2.       The semiconductor package of claim 1, said backside metallization layer  
2           including three layers including an adhesion/barrier layer, a wetting layer, and a protection layer.

1           3.       The semiconductor package of claim 2, said adhesion/barrier layer formed of a  
2           material selected from the group consisting of Ti, TiN, Ta, and TaN.

1           4.       The semiconductor package of claim 2, said wetting layer formed of a material  
2           selected from the group consisting of NiV and Ni.

1           5.       The semiconductor package of claim 2, said protection layer formed of a  
2           material selected from the group consisting of Au, Pt and Pd.

1           6.       The semiconductor package of claim 1, said solder portion including AuSn  
2           solder.

1           7.       The semiconductor package of claim 6 wherein said solder portion includes  
2           either separate Au and Sn layers or a single eutectic AuSn layer.

1           8.       The semiconductor device of claim 7 wherein a thickness of Au layer and Sn  
2           layer is formed so that an overall Au-to-Sn ratio by weight is 80 to 20.

1           9.       The semiconductor package of claim 1, said thermal interface layer including a  
2           barrier layer disposed between the solder portion and the integrated heat spreader.

1           10.     The semiconductor package of claim 9 wherein said barrier layer is formed of  
2     Ni.

1           11.     The semiconductor package of claim 1, wherein said backside metallization  
2     layer includes an adhesion/barrier layer, a wetting layer, and a protection layer, and said thermal  
3     interface layer includes a solder portion including gold (Au) and tin (Sn) together with a barrier  
4     layer formed of nickel (Ni) disposed between the solder portion and the integrated heat spreader.

1           12.     A method for forming a semiconductor package having a semiconductor die  
2     coupled to an integrated heat spreader, the method comprising:  
3             forming a metallization layer on a backside of the semiconductor die;  
4             forming a thermal interface portion on a topside of the integrated heat spreader, said  
5     thermal interface portion including a solder layer; and  
6             forcing together under load and heat the metallization layer and the solder layer  
7     without flux to bond the semiconductor die to the integrated heat spreader.

1           13.     The method of claim 12, further including heating the package to above 300°C  
2     for a package heating time of between about 1 and 30 minutes and ramping down the  
3     temperature lower than about 100°C per minute.

1           14.     The method of claim 13, wherein the package heating time is between about 2  
2     and 3 minutes.

1           15.     The method of claim 13, wherein the temperature is ramped down approximately  
2     30°C per minute.

1           16.     The method of claim 12 further including reacting the solder layer with the  
2     metallization layer to form bonded intermetallic layers.

1           17.     The method of claim 16, wherein the solder layer includes gold (Au) and tin (Sn)  
2     and the metallization layer includes a protection layer formed of a material selected from the  
3     group consisting of gold (Au), Platinum (Pt), and Palladium (Pd) and a wetting layer formed of  
4     a material selected from the group consisting of nickel-vanadium (NiV) and nickel (Ni).

1           18.     The method of claim 17, wherein the solder layer reacts with the protection layer  
2     and wetting layer to form intermetallics using a fluxless bonding approach.

1           19.     The method of claim 18, wherein the solder layer includes gold (Au) and tin  
2     (Sn), the protection layer is gold (Au) and the wetting layer is nickel (Ni) where the intermetallic  
3     formed is Au-Sn-Ni.

1           20.     The method of claim 12 wherein the metallization layer includes an  
2     adhesion/barrier layer, a wetting layer, and a protection layer.

1           21.     The method of claim 12, further including bonding the die of the semiconductor  
2     package onto an organic printed circuit board substrate.

1           22.     The method of claim 12 wherein forcing the metallization layer and fluxless  
2     solder layer together under load and heat includes placing the package within a reflow oven  
3     purged with N<sub>2</sub>.

1           23.     The method of claim 12 wherein the step of forcing the metallization layer and  
2     fluxless solder layer together under load and heat further includes:

3                 resting the integrated heat spreader on a carrier with the fluxlessly-capable solder layer  
4     exposed;

5                 placing the die on top of the integrated heat spreader with the metallization layer in  
6     contact with the fluxlessly-capable solder layer;

7                 holding the die onto the integrated heat spreader using a downward force on the  
8     package; and

9                 heating the package within a reflow oven purged with N<sub>2</sub>.

10  
1           24.     The method of claim 23 wherein the downward force includes a clip holding the  
2     die onto the integrated heat.

1           25.     The method of claim 23 further including ramping down the heat applied to the  
2     package after heating the package.

1           26.     The method of claim 23 wherein the reflow oven used for heating the package  
2 includes multiple zones each with independent temperature controls.

1           27.     The method of claim 26, said reflow oven multiple zones have a maximum  
2 temperature of 400°C.